1. A method of forming dual gates in the fabrication of an integrated circuit device comprising:

growing a first gate dielectric layer overlying a substrate;

depositing a polysilicon layer overlying said first gate dielectric layer;

patterning said polysilicon layer to form first NMOS gates;

thereafter growing a second gate dielectric layer overlying said substrate;

depositing a polysilicon-germanium layer overlying said second gate dielectric layer and said first gates;

planarizing said polysilicon-germanium layer and said first gates to a uniform thickness; and

thereafter patterning said polysilicon first gates and said polysilicon-germanium layer to form second NMOS polysilicon gates and PMOS polysilicon-germanium gates in the fabrication of an integrated circuit device.

2. The method according to Claim 1 wherein said first gate dielectric layer comprises an oxide grown to a thickness of between about 12 and 65 Angstroms.

3. The method according to Claim 1 wherein said polysilicon layer is deposited to a thickness of between

about 1500 and 2000 Angstroms.

4. The method according to Claim 1 wherein said second gate dielectric layer is an oxide grown to a thickness of between about 12 and 20 Angstroms.

5. The method according to Claim 1 wherein said polysilicon-germanium layer is deposited to a thickness of between about 1700 and 2000 Angstroms.

6. The method according to Claim 1 wherein said uniform thickness is between about 1500 and 2000 Angstroms.

7. A method of forming dual gates in the fabrication of an integrated circuit device comprising:

providing a thick device area and a thin device area of a substrate;

growing a first gate dielectric layer overlying said substrate in each of said device areas;

depositing a polysilicon layer overlying said first gate dielectric layer;

patterning said polysilicon layer to form first NMOS and PMOS gates in said thick device area and to form first NMOS gates in said thin device area;

growing a second gate dielectric layer overlying

said substrate;

depositing a polysilicon-germanium layer overlying said second gate dielectric layer and said first gates;

planarizing said polysilicon-germanium layer and said first gates to a uniform thickness; and

thereafter patterning said polysilicon first gates and said polysilicon-germanium layer to form second NMOS and PMOS polysilicon gates in said thick device area, second NMOS polysilicon gates in said thin device area, and second PMOS polysilicon-germanium gates in said thin device area in the fabrication of an integrated circuit device.

8. The method according to Claim 7 wherein said first gate dielectric layer is an oxide grown to a thickness of between about 12 and 65 Angstroms.

9. The method according to Claim 7 wherein said polysilicon layer is deposited to a thickness of between about 1500 and 2000 Angstroms.

10. The method according to Claim 7 wherein said second gate dielectric layer is an oxide grown to a thickness of between about 12 and 20 Angstroms.

11. The method according to Claim 7 wherein said polysilicon-germanium layer is deposited to a thickness of between about 1700 and 2000 Angstroms.

12. The method according to Claim 7 wherein said uniform thickness is between about 1500 and 2000 Angstroms.

13. The method according to Claim 7 wherein said NMOS and PMOS polysilicon gates in said thick device area have a width of between about 2400 and 3000 Angstroms.

14. The method according to Claim 7 wherein said NMOS polysilicon gates in said thin device area have a width of between about 700 and 850 Angstroms.

15. The method according to Claim 7 wherein said PMOS polysilicon-germanium gates in said thin device area have a width of between about 700 and 850 Angstroms.

16. A CMOS integrated circuit device comprising:

NMOS and PMOS polysilicon gates in a thick device area of a wafer;

NMOS polysilicon gates in a thin device area of said wafer; and

PMOS polysilicon-germanium gates in said thin

device area of said wafer.

17. The device according to Claim 16 wherein said NMOS and PMOS polysilicon gates in said thick device area comprise:

a gate oxide layer having a thickness of between about 45 and 65 Angstroms; and

a polysilicon layer having a thickness of between about 1500 and 2000 Angstroms and having a width of between about 2400 and 3000 Angstroms.

18. The device according to Claim 16 wherein said NMOS polysilicon gates in said thin device area comprise:

a gate oxide layer having a thickness of between about 12 and 20 Angstroms; and

a polysilicon layer having a thickness of between about 1500 and 2000 Angstroms and having a width of between about 700 and 850 Angstroms.

19. The device according to Claim 16 wherein said PMOS polysilicon-germanium gates in said thin device area comprise:

a gate oxide layer having a thickness of between about 12 and 20 Angstroms; and

a polysilicon-germanium layer having a thickness of

between about 1500 and 2000 Angstroms and having a width of between about 700 and 850 Angstroms.